IN THE CLAIMS

The following claim set replaces all prior versions, and listings, of claims in the application:

Please cancel without prejudice claims 5, 6, 13, 14 through 37 and 40, amend claims 1 through 4, 7 through 12, 38, 39, 41 through 45 and 48 through 50 and add newly written claims 51 to 54 as follows:

1. *(Twice Amended)* A photodetector circuit comprising:

a photodiode detector, said photodetector having a PN structure with p-type and n-type active regions; ~~and~~

~~an associated~~ a readout circuit, said readout circuit ~~incorporates~~ at least partly incorporated in a CMOS component and having ~~supporting at least one deposited epitaxial layer which is one of said active regions of the photodiode detector and including~~ a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and

a deposited epitaxial layer supported by said CMOS component, said epitaxial layer providing only one of said active regions, said photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

2. *(Twice Amended)* A photodetector circuit according to Claim 1 wherein the CMOS component comprises a substrate supporting and insulated from said CMOS ~~circuitry~~ circuit, the photodiode detector is operable in current multiplication mode and

the ~~at least one~~ epitaxial layer is deposited upon the substrate.

3. *(Twice Amended)* A photodetector circuit according to Claim 39, wherein the ~~at least one~~ epitaxial layer provides a high field region.

4. *(Twice Amended)* A photodetector circuit according to Claim 2 wherein the photodiode detector is an avalanche photodiode and said photodiode active regions comprises a first active region incorporated in the substrate, and the ~~at least one~~ epitaxial layer is a layer deposited upon the first active region and provides a second active region of the photodiode.

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5. Cancelled

6. Cancelled

7. *(Twice Amended)* A photodetector circuit according to Claim 1 wherein said readout circuit is arranged to provide said photodiode detector with a logarithmic response to incident radiation.

8. *(Twice Amended)* A photodetector circuit according to Claim 1, wherein said readout circuit incorporates parasitic photodiodes, arranged ~~to contribute~~ in series with said readout circuit, for contributing to circuit output in response to incident radiation.

9. *(Twice Amended)* A photodetector circuit according to Claim 1, wherein said readout circuit includes an amplifier arranged ~~to provide~~ in a feedback loop for providing

feedback to stabilise photodiode detector bias voltage.

10. *(Twice Amended)* A photodetector circuit according to Claim 9, wherein the amplifier is arranged to amplify an output signal from the photodiode detector and to provide feedback to bias a load transistor ~~(ML5)~~ in series with the photodiode detector.

11. *(Previously Amended)* A photodetector circuit according to Claim 10, wherein the amplifier is a push-pull amplifier.

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12. *(Twice Amended)* A photodetector circuit according to Claim 10, wherein said readout circuit includes a cascode transistor arranged to reduce Miller Effect capacitance in the amplifier.

13. *through 37 Cancelled*

38. *(Amended)* A photodetector circuit comprising:

a photodiode detector, said photodetector having a PIN structure, said structure having ~~three~~ first, second and third active regions, one active region p-type, one active region substantially undoped and one active region n-type; ~~and~~

~~an associated~~ a readout circuit, said readout circuit ~~incorporates~~ at least partly incorporated in a CMOS component and having ~~supporting at least one deposited epitaxial layer which is one of said active regions of the photodiode detector and including~~ a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and

a deposited epitaxial layer supported by said CMOS component, said epitaxial layer providing only one of said active regions, said photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

39. *(Amended)* A photodetector circuit according to Claim 38 wherein the readout circuitry incorporates CMOS circuitry, the CMOS component comprises a substrate supporting and insulated from said CMOS circuitry, the photodiode detector is operable in current multiplication mode and the ~~at least one~~ epitaxial layer is deposited upon the substrate.

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40. *Cancelled*

41. *(Amended)* A photodetector circuit according to Claim 39, wherein the epitaxial layer comprises ~~two~~ a first epitaxial layer supporting a second epitaxial layer, ~~layers~~ said first epitaxial layer providing said second active region and said second epitaxial layer, on said first epitaxial layer, comprising said third active region ~~regions~~ of the photodiode, ~~the second region is upon the first region and the third region is upon the second region, the first and third regions are of mutually opposite conductivity type, the second region is substantially undoped and the third region is an epitaxial layer~~.

42. *(Amended)* A photodetector circuit according to Claim 41, wherein the third ~~avalanche photodiode~~ active region is electrically connected to the guard ring and has like potential therewith during circuit operation.

43. *(Amended)* A photodetector circuit according to Claim 38, wherein said readout circuit includes at least one circuit element arranged to provide said photodiode detector with a logarithmic response to incident radiation.

44. *(Amended)* A photodetector circuit according to Claim 38, wherein said readout circuit incorporates parasitic photodiodes arranged in series with said readout circuit, for contributing ~~to contribute~~ to circuit output in response to incident radiation.

45. *(Amended)* A photodetector circuit according to Claim 38, wherein said readout circuit includes an amplifier arranged ~~to provide~~ in a feedback loop for providing feedback to stabilise photodiode detector bias voltage.

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46. *(Previously New)* A photodetector circuit according to Claim 45, wherein the amplifier is arranged to amplify an output signal from the photodiode detector and to provide feedback to bias a load transistor in series with the photodiode detector.

47. *(Previously New)* A photodetector circuit according to Claim 46, wherein the amplifier is a push-pull amplifier.

48. *(Amended)* A photodetector circuit according to Claim 46, wherein said readout circuit includes a cascode transistor arranged to reduce Miller Effect capacitance in the amplifier.

49. *(Amended)* A photodetector circuit according to Claim 38, wherein the CMOS

component is a substrate supporting and insulated from CMOS circuitry, the photodiode detector comprises a ~~first~~ region of one conductivity type incorporated in the substrate, and the ~~at least one~~ epitaxial layer comprises ~~two~~ a first epitaxial layer supporting a second epitaxial layer, ~~layers~~ one of ~~which~~ said epitaxial layers is substantially undoped and the other of ~~which~~ said epitaxial layers is of opposite conductivity type to that of the ~~first~~ region incorporated in the substrate, the ~~first~~ region in the substrate and the two epitaxial layers ~~being configured as~~ comprising a PIN diode.

50. *(Amended)* A photodetector circuit according to Claim 49, wherein the undoped epitaxial layer is one of a SiGe alloy ~~or is~~ and a quantum well structure of the $Si_{1-x}Ge_x$ material system where the value of the compositional parameter x changes between successive layers.

--51. *(New)* An array of photodetector circuits, each photodetector circuit comprising:

a photodiode detector, said photodiode detector having a PN structure with p-type and n-type active regions;

a readout circuit, said readout circuit being at least partly incorporated in a CMOS component and having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and

a deposited epitaxial layer supported by the CMOS component, the epitaxial layer

providing only one of said active regions of the photodiode detector, the photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

52. *(New)* An array of photodetector circuits, each photodetector circuit comprising:

a photodiode detector, said photodiode detector having PIN structure, said structure having three active regions, one active region p-type, one active region substantially undoped and one active region n-type;

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a readout circuit, said readout circuit being at least partly incorporated in a CMOS component and having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and

a deposited epitaxial layer supported by the CMOS component and providing only one of said active regions of the photodiode detector, the photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

53. *(New)* A method of making a photodetector circuit comprising the steps of:

forming at least part of a readout circuit as a CMOS component, the readout circuit having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and a photodiode detector,

forming a deposited epitaxial layer supported by the CMOS component to produce a photodiode detector having a PN structure with p-type and n-type active regions, the epitaxial layer providing only one of said active regions, the photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.

54. *(New)* A method of making a photodetector circuit comprising the steps of:

forming at least part of a readout circuit as a CMOS component, the readout circuit having a guard ring delimiting and surrounding the photodiode detector for enhancing electric field uniformity and inhibiting breakdown; and a photodiode detector,

forming a deposited epitaxial layer supported by the CMOS component to produce a photodiode detector having PIN structure with three active regions, one active region p-type, one active region substantially undoped and one active region n-type, the epitaxial layer providing only one of said active regions, the photodiode detector, in response to said only one active region, having a gradual knee in a current-voltage characteristic.--